



SHEET 1 OF 1

INFORMATION DISCLOSURE  
CITATION IN AN  
APPLICATION

(PTO-1449)

ATTY. DOCKET NO.  
60188-137SERIAL NO.  
10/038,613APPLICANT  
Toru IWATA, et al.FILING DATE  
January 08, 2002GROUP  
2631

## U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
99		US 6,236,696 B1	05/22/2001	Aoki et al.	(Corresponds with JP 10-327068)
		US			
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		US			

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## FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code - Number - Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
99		JP 11-243327	09/07/1999	HITACHI LTD		JAPAN (w/Abstract and Partial English Translation)	
99		JP 61-70830	04/11/1986	HITACHI LTD.		JAPAN(w/English Abstract)	
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99		JP 5-136635	06/01/1993	INTERNATL BUSINESS MACH CORP <IBM>		JAPAN(w/English Abstract)	
99		JP 8-237117	09/13/1996	NEC CORP		JAPAN(w/English Abstract)	
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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  (PTO-1449)				ATTY. DOCKET NO. <b>60188-137</b>		SERIAL NO.	
				APPLICANT <b>Toru IWATA, et al.</b>			
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JCS97 U.S. PTO  
 10/038613  
  
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EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
QG	6,064,248	5/16/2000	Seki			

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
QG	D.H. Wolaver, "Phase-Locked Loop Circuit Design", Section 10-2, pp. 213-216, Prentice Hall (1991)
QG	R. Gu, et al., "A 0.5-3.5Gb/s Low-Power Low-Jitter Serial Data CMOS Transceiver", ISSCC Digest of Technical Papers, pp. 352-353, Feb. 1999.

EXAMINER	DATE CONSIDERED <b>4/7/05</b>
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